ABSTRACT

A Time Division Multiple Access (TDMA) mobile station architecture consuming less power and random access memory (RAM) is presented herein. The mobile station includes a system timer coprocessor with a microsequencer for executing frame programs stored in microcode random access memory. The microsequencer operates in a mode, wherein the microcode random access memory is divided into two regions. The frame programs are stored in a particular one of the two regions in an alternating manner.